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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/254,939	MIURA ET AL.	
	Examin r	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communicati n appears n th cover sheet with the c rrespondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9,10,12,13,15,17-39 and 41-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9,10,12,13,15,17-39 and 41-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Status of the Claims

1. Amendment filed June 5, 2003 has been entered as Paper No. 29. Claims 1, 2, 4, 5, 9, 10, 15, 41, 43, 45-47 have been amended. Claims 54 and 55 have been added. Claims 1-6, 9, 10, 12, 13, 15, 17-39 and 41-55 are pending.

Response to Amendment

2. The amendment filed June 5, 2003 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "performing oxidation of said semiconductor substrate **having said polished surface**".

Note that, at best, page 7, 13 and 14 of the originally filed specification discloses: The buried insulating film is etched back by chemical-mechanical polishing (CMP) or dry etching, lines 10-12 and 15-17, respectively.

The specification fails to support the newly added limitation.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-6, 9, 10, 12, 13, 15, 17-39 and 41-53 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains

subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "performing oxidation of said semiconductor substrate **having said polished surface**" in the application as filed. .

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims **1**, **9**, **10**, 12, 13, **15**, 17-20, 30-39, **41**, 42, 46-49 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta et al. (U.S. Patent No. 5,646,063) in view of Otsu (U.S. Patent No. 5,236,861) all of record.

With respect to claim **1**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (12);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (12), the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in the semiconductor substrate (12), exposed in the trench;

(d) burying a buried insulating film (60) into the trench (44) so oxidized;

(e) after burying the buried insulating film (60), removing the insulating film (60) on the oxidation prevention film (18), by chemical mechanical polishing (CMP), thereby forming a polished surface;

(f) after the removing, performing oxidation of the semiconductor substrate, so as to oxidize only a portion of the semiconductor substrate (14) at the upper end portion of the trench, and not substantially at other portion of the semiconductor substrate lining the trench, so as to provide a curvature of the upper end portion of the trench;

(g) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(h) after eliminating, forming a gate oxide film (135). (See Figs. 1-9).

Thus, Mehta is shown to teach all the features of the claim with the exception of performing oxidation of the semiconductor substrate having the polished surface.

However, Otsu teaches: performing oxidation of the semiconductor substrate (1) having a polished surface, so as to oxidize only a portion of the semiconductor substrate (1) at the upper end portion of the trench (6). (See Fig. 3E).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to perform oxidation of the semiconductor substrate (14) following the CMP as taught by Otsu to provide curvature at the upper end portion of the trench with less process steps.

With respect to claim **9**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (12);

(b) forming trench regions (44) in the substrate from the circuit formation surface thereof;

(c) performing a first oxidation to form an oxide film (56) on the trench regions (44) formed in step (b), and

(d) forming an insulating film (60) inside the oxidized trench regions (44) so as to completely fill them, thereby forming completely filled trench regions, and forming the insulating film (60) on the oxidation prevention film (18),

(e) removing the insulating film (60) formed on the oxidation prevention film (18) by chemical mechanical polishing (CMP), thereby forming a polished surface;

(f) after the removing, performing a second oxidation, of the semiconductor substrate, so as to selectively oxidize only an opening side of the completely filled trench regions in the substrate; and

(g) after performing the second oxidation, removing the oxidation prevention film (18), and forming a gate oxide film (135). (See Figs. 1-9).

With respect to performing a second oxidation of the semiconductor substrate having the polished surface, the same reasoning as that of claim 1 is also applied here.

With respect to claim **10**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in the semiconductor substrate, exposed in the trench (44);

(d) burying a buried insulating film (60) into the trench so oxidized, the insulating film also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18) by CMP, thereby forming a polished surface;

(f) after removing, performing oxidation of the semiconductor substrate (14), so as to oxidize only apportion of the semiconductor substrate, at the upper end portion of the trench and not substantially at other portions of the semiconductor substrate lining the trench, to provide the upper end portions with a curvature; and

(g) removing the oxidation prevention film (18) formed on the circuit formation surface of the semiconductor substrate. (See Figs. 1-9).

With respect to performing a second oxidation of the semiconductor substrate having the polished surface, the same reasoning as that of claim 1 is also applied here.

With respect to claim 12, providing curvature of Mehta includes forming a well known bird's beak at the upper end portion of the trench. (see Fig. 1).

With respect to claim 13, the providing the curvature of Mehta is formed such that an angle (θ) between the circuit formation surface of the semiconductor substrate and a side surface of the semiconductor substrate forming the trench is within a range of $90° < \theta > 180°$.

With respect to claim **15**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in the semiconductor substrate, exposed in the trench (44), so as to provide the upper end portion of the trench with a curvature;

(d) burying a buried insulating film (60) into the trench so oxidized, the insulating also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), having the buried insulating film (60) in the trench, by CMP thereby forming a polished surface;

(f) after removing, performing thermal oxidation of the semiconductor substrate (14) only at the upper portion end portion of the trench (44), to increase the curvature provided in step (c); and

(g) removing the oxidation prevention film (18) formed on the circuit formation surface of the semiconductor substrate (12). (See Figs. 1-9).

With respect to performing a second oxidation of the semiconductor substrate having the polished surface, the same reasoning as that of claim 1 is also applied here.

With respect to claim **41**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (12);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (12), the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in the semiconductor substrate, exposed in the trench (44), forming a curvature of the upper end portion of the trench (44);

(d) burying a buried insulating film (60) into the trench (200) so oxidized, the insulating film also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a polished surface;

(f) after the removing, performing selective oxidation of the semiconductor substrate (14) at the upper end portion so as to provide an increased curvature of the upper end portion of the trench (44) as compared with the curvature formed in step (c);

(g) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(h) after the eliminating, forming a gate oxide film (135). (See Figs. 1-9).

With respect to performing a second oxidation of the semiconductor substrate having the polished surface, the same reasoning as that of claim 1 is also applied here.

With respect to claim **46**, as best understood by the examiner, Mehta '063 teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench regions (44) in the substrate from the circuit formation surface thereof;

(c) performing a first oxidation to form an oxide film (56) on the trench regions formed in step (b), so as to provide a curvature at an opening side of the trench regions (44); and

(d) forming an insulating film (60) inside the oxidized trench regions (44) so as to completely fill them, the insulating film (60) also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a polished surface;

(f) after the removing, performing a selective second oxidation of the semiconductor substrate (14) to selectively oxidize the opening side of the completely filled trench regions (44)

in the substrate (12) so as to provide an increased curvature at the opening side as compared to the curvature provided in step (c); and

(g) after performing the second oxidation, removing the oxidation prevention film (18) and forming a gate oxide film (135). (See Figs. 1-9).

With respect to performing a second oxidation of the semiconductor substrate having the polished surface, the same reasoning as that of claim 1 is also applied here.

With respect to claim **47**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined positions of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portions thereof extending to the circuit formation surface of the semiconductor substrate (14);

(c) oxidizing a trench portions formed in the semiconductor substrate, exposed in the trenches (44), there by providing the upper end portion of the trench with a curvature;

(d) burying a buried insulating film (60) into the trench (44) so oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a polished surface;

(f) after the removing, providing the upper end portion of the trench (44) with an increased radius of curvature, as compared with the radius of curvature provided in step (c), by performing selective oxidation of the upper end portion of the trench (44) of the semiconductor substrate; and

(g) removing the oxidation film prevention film (18) formed on the circuit formation surface of the semiconductor substrate (12). (See Figs. 1-9).

With respect to performing a second oxidation of the semiconductor substrate having the polished surface, the same reasoning as that of claim 1 is also applied here.

With respect to claim 17, the oxidizing of Mehta is thermal oxidation, so as to provide the curvature.

With respect to claims 18-20 and 30-38, the buried insulating film of Mehta is silicon oxide, deposited by CVD.

With respect to claim 39, the step (f) of removing the oxidation prevention film (18) of Mehta is performed after the performing thermal oxidation.

With respect to claims 42 and 48, step (g) of Mehta is performed after step (f).

With respect to claims 49 and 52, the oxidation prevention film (18) of Mehta is eliminated after the oxidizing only a portion of the semiconductor substrate.

5. Claims **2**, 3, **5**, 6, 21-23, 27-29, **43**, 44 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta '063 in view of Yuzuriha (JP-01-107554) and Otsu '861, all of record.

With respect to claims **2** and **43**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(c) forming trenches (44) having a predetermined depth in the semiconductor substrate;

(d) oxidizing trench portions formed in the semiconductor substrate (14), exposed in the trenches (44);

(e) burying a buried insulating film (60) into the trench so oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(f) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a polished surface;

(g) after the removing, performing oxidation of the semiconductor substrate, so as to oxidize only a portion of the semiconductor substrate (14) extending from the corners, and not substantially at other portions of the semiconductor substrate lining the trenches, after the removing , so as to increase the curvature of the trenches corner;

(h) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(i) after eliminating, forming a gate oxide film (135). (See Figs. 1-9).

Thus, Mehta is shown to teach all the features of the claim with the exception of forming the trenches using two steps etching and performing oxidation of the semiconductor substrate having the polished surface.

However, Yuzuriha '554 teaches forming a trench using two steps etch:

(b) forming shallow trenches having a radius curvature at the corners in a desired position of the circuit formation surface of a semiconductor substrate (1);

(c) forming trench having a predetermined depth to the shallow trenches having a radius of curvature so formed. (See Figs. 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trenches of Mehta using two etching steps as taught by Yuzuriha to reduced leakage current. (See Constitution).

Further, Otsu teaches: performing oxidation of the semiconductor substrate (1) having a polished surface, so as to oxidize only a portion of the semiconductor substrate (1) at the upper end portion of the trench (6). (See Fig. 3E).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to perform oxidation of the semiconductor substrate (14) of Mehta following the CMP as taught by Otsu to provide curvature at the upper end portion of the trench with less process steps.

With respect to claim **5**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(c) forming trenches (44) having a predetermined depth in the semiconductor substrate;

(d) oxidizing trench portions formed in the semiconductor substrate (14), exposed in the trenches (44);

(e) burying a buried insulating film (60) into the trench so oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(f) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a polished surface;

(g) after the removing, performing oxidation of the semiconductor substrate (14), so as to oxidize only a portion of the semiconductor substrate extending from the corners, and not substantially at other portions of the semiconductor substrate lining the trenches, so as to increase the curvature of the trenches corner;

(h) removing the oxidation prevention film (18) formed on the circuit formation surface of the semiconductor substrate (12); and

(i) after the oxidizing the semiconductor substrate (12), forming a gate oxide film (135). (See Figs. 1-9).

Regarding the formation of shallow trenches having radius of curvature and performing oxidation of the semiconductor substrate having the polished surface, the similar reasoning as that of claims **2** and **43** is also applied here.

With respect to claims 3, 6, the step for forming shallow trenches of Yuzuriha is carried out by isotropic etching and the step of forming trenches is carried out by anisotropic etching to a predetermined depth.

With respect to claims 21-23, 27-29, the buried insulating film of Mehta is silicon oxide, deposited by CVD.

With respect to claim 44, step (h) of Mehta is performed after step (g).

With respect to claim 51, the oxidation prevention film (18) of Mehta '063 is removed after the oxidizing only portion of the semiconductor substrate.

6. Claims **4**, 24-26, **45**, 50 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta (U.S. Patent No. 5,679,599) in view of Otsu '861, all of record .

With respect to claim **4**, as best understood by the examiner, Mehta '599 teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (120) on a circuit formation surface of a semiconductor substrate (100);

(b) forming trench having a predetermined depth at a desired positions of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion (185) not covered by the oxidation prevention film (120);

(c) oxidizing trench portions formed in the semiconductor substrate, exposed in the trench;

(d) burying a buried insulating film (230) into the trench so oxidized, the insulating film also being formed on the oxidation prevention film (120);

(e) removing the insulating film (230) on the oxidation prevention film (120), by CMP, thereby forming a polished surface;

(f) after the removing, performing oxidation of the semiconductor substrate, so as to oxidize only a portion of the semiconductor substrate at the upper end portion of the trenches, and not substantially at other portions of the semiconductor substrate lining the trenches, the upper end portions not covered by the oxidation prevention film being oxidized;

(g) removing the oxidation preventing film (120) formed on the circuit formation surface of the semiconductor substrate; and

(h) after the oxidizing the semiconductor substrate, forming a gate oxide film. (See Figs. 11-18).

Thus, Mehta '599 is shown to teach all the features of the claim with the exception of explicitly disclosing the removal of the oxidation preventing film (120); forming a gate oxide film and performing oxidation of the semiconductor substrate having the polished surface.

However, the teaching of Mehta includes forming the isolation structure in an integrated circuit such as CMOS and memory devices, as shown in Fig. 5.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the oxidation prevention film (120) and form the gate oxide on the

semiconductor substrate of Mehta at the completion of the isolation structures since the process is well known and within the ability of a skill worker in the art prior to the forming the CMOS and the memory devices.

Further, Otsu teaches: performing oxidation of the semiconductor substrate (1) having a polished surface, so as to oxidize only a portion of the semiconductor substrate (1) at the upper end portion of the trench (6). (See Fig. 3E).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to perform oxidation of the semiconductor substrate (14) following the CMP as taught by Otsu to provide curvature at the upper end portion of the trench with less process steps.

With respect to claims 24-26, the buried insulating film (230) of Mehta is silicon oxide, deposited by CVD.

With respect to claim **45**, as best understood by the examiner, Mehta '599 teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (120) on a circuit formation surface of a semiconductor substrate (100);

(b) forming a trench (200) having a predetermined depth at a desired positions of the circuit formation surface of the semiconductor substrate (100), the trench having an upper end portions not covered by the oxidation prevention film (120);

(c) oxidizing a trench portions formed in the semiconductor substrate (100), exposed in the trenches (200), so as to provide a curvature at the upper end portions of the trench (200);

(d) burying a buried insulating film (230) into the trench (200) so oxidized, the insulating film (230) also being formed on the oxidation prevention film (120);

(e) removing the insulating film (230) on the oxidation prevention film (120), by CMP, thereby forming a polished surface;

(f) performing selective oxidation of the semiconductor substrate (100) after the insulating film (230) formed on the oxidation prevention film (120) is removed, the upper end portion not covered by the oxidation prevention film (120) being oxidized;

(g) removing the oxidation prevention film (120) formed on the circuit formation surface of the semiconductor substrate; and

(h) after oxidizing the semiconductor substrate, forming a gate oxide film. (See Figs. 11-18).

Regarding the removal of the oxidation preventing film (120); forming a gate oxide film and performing selective oxidation of the semiconductor substrate having the polished surface, the similar reasoning as that of claim **4** is also applied here.

With respect to claims 50 and 53, the oxidation prevention film (120) of Mehta '599 is removed after the oxidizing only portion of the semiconductor substrate.

7. Claims **54** and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta '063 in view of Yuzuriha '554.

With respect to claim **54**, Mehta '063 teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate (14), trench (44) being formed by anisotropic etching the semiconductor substrate (14);

(c) oxidizing the trench portions formed in the semiconductor substrate (14), exposed in the trenches (44);

(d) burying a buried insulating film (60) into the trench so oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(e) after burying the buried insulating film(60), performing an additional thermal oxidation so as to selectively oxidize the semiconductor substrate at the upper end portion of the trench (44);

(f) after burying the buried insulating film (60), removing the insulating film (60) on the oxidation prevention film (18);

(g) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(h) after eliminating, forming a gate oxide film (135). (See Figs. 1-9).

Thus, Mehta is shown to teach all the features of the claim with the exception of forming the trenches using two steps etching.

However, Yuzuriha '554 teaches forming a trench using two steps etching by first using isotropic etch, so as to form a radius of curvature (3a) in a proximity of the upper end portion, and by a second using anisotropic etching. (See Figs. 1A-C).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trenches (44) of Mehta using two etching steps as taught by Yuzuriha to reduced leakage current. (See Constitution).

With respect to claim 55, performing an additional thermal oxidation of Mehta is performed after removing the insulating film (60) on the oxidation prevention film (18).

Response to Arguments

8. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

The Amendment to the claims have altered the scope of the claims. The Office Action based on the amended claims constitutes new ground of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

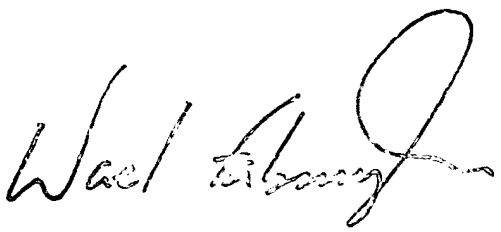
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
June 27, 2003



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